IN THE SPECIFICATION:

Please amend Paragraph [0021] as follows:

[0021] The voltage divider 3 comprises a first resistor [[3a]] 3b and a second resistor [[3b]] 3a connected in serial to the first resistor [[3a]] 3b. The first resistor [[3a]] 3b is connected to the input terminal 31, which is coupled to the output 22 of the voltage source 2, while the second resistor 3a is grounded. A node common to the first resistor 3a and the second resistor [[3b]] 3a is guided to the output terminal 32 of the voltage divider 3 that is coupled to the first input terminal 41 of the controller 4. An exemplary resistance is 620 kΩ and 20 kΩ for the first resistor [[3a]] 3b and the second resistor [[3b]] 3a, respectively.

Please amend Paragraph [0028] as follows:

[0028] In FIG. 1, the bias voltage applied to the APD 1 is calculated as,

$$V_{apd} = V_{ref} * (R_{3a} + R_{3b}) / [[R_{3b}]]\ \underline{R_{3a}},\qquad (2)$$

$$V_{ref} = 2.5 - R_g/255,\qquad (3)$$